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Low-Noise Amplifier Designs at 5 GHz

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Abstract

Two different designs of a low-noise amplifier (LNA) at 5 GHz are presented in this paper. The first design uses lumped elements for implementing the matching networks. The second design utilizes distributed element matching networks using microstrip lines. It is shown that the design using lumped element matching networks has difficulties to achieve high performance at a frequency of above 5 GHz and that distributed matching circuits are more adequate compared to the lumped element solution. Experimental results confirm the simulation results based on the LNA design with distributed matching networks.

INTRODUCTION

The low-noise amplifier (LNA) is a key block in a receiver, setting the receiving sensitivity of the entire system. The main requirements of the LNA are the lowest possible noise figure (NF) with a reasonable gain. The general topology of the LNA consists of three stages: the input matching network (IMN), the amplifier itself and the output matching network (OMN). In addition to selecting the appropriate active component, the IMN and OMN are critical factors in achieving the specified overall amplifier performances.

The purpose of this paper is to present two different designs of a LNA at 5 GHz. The circuit design starts from MAXIM's MAX2649 amplifier and uses the Advanced Design System (ADS) 2003C tool provided by Agilent Technologies Inc. The first design uses discrete components, modeled as lumped elements for implementing the matching networks. The second design utilizes microstrip lines, modeled as distributed elements in ADS. The component parameter variations and the PCB manufacture process variations are included in the simulation set-up. Finally, LNA samples are fabricated and measured using the Rhode&Schwarz vector network analyzer ZVM.

CIRCUIT DESIGN

The LNA presented in this paper is a part of a radio frequency (RF) front-end module at 5 GHz (Fig. 1). The LNA specifications are derived from the top-down design of the entire front-end [1]:

- Frequency range: 5.15-5.35 GHz
- Noise Figure ≤ 2.1 dB
- Gain > 11 dB
- Operating between 50 Ω terminations

The active device (MAX2649) is described in the ADS design flow as a two-port network in the form of the Touchstone format file (*.s2p).

Both S-parameters and noise parameters of the active device are included in this file and are used for noise and power gain matching as well as for stability analysis of the LNA.

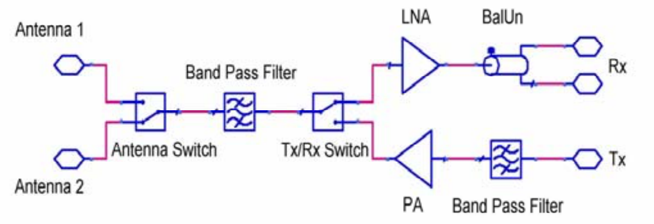

Fig. 1. Block diagram of the 5 GHz RF front-end.

The substrate used is a double layer PCB with the Rogers material RO4350B. The PCB parameters are presented in Table 1. For the chosen PCB manufacture process the minimum width of the microstrip lines is 75 µm, with a specified tolerance of ±10%.

A. Stability Analysis

Two problems appear when designing a LNA:

1) Achieving the specified noise figure, while keeping the input power matching (the amplifier gain) as good as possible.

2) Achieving stability without worsening too much the noise figure and the gain of the amplifier.

Besides the optimal noise figure, the stability of the amplifier is an important aspect in every RF design. Here, the chosen stabilization method is a shunt resistor at the output. Simulation results presented in Fig. 2 show that the stabilization method increases the minimum noise figure, NF_{min}, with 0.1 dB over the entire frequency band.

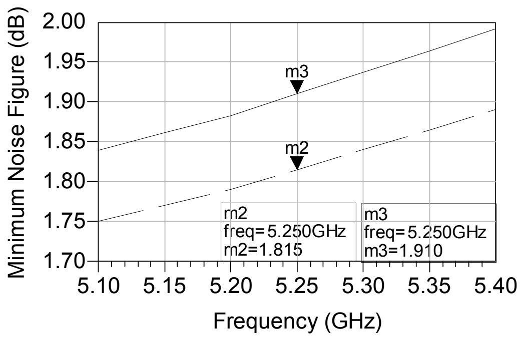

Fig. 2. Simulated minimum noise figure, NF_{min}, without and with the stabilization resistor, marked with m2 and m3, respectively.

TABLE I

PCB PROCESS PARAMETERS

Material	RO4350B
Dielectric thickness	0.254 mm
Dielectric constant	3.48 ± 0.05
Dissipation factor	0.0037
Metal thickness	0.045 mm
Metal conductivity	5.8 x 107 S/m
Surface roughness	0.001 mm

B. Input and Output Matching Networks for Minimum Noise Figure

The stabilized amplifier was simulated and the simulation results indicate a minimum noise figure, NF_{min}, equal to 1.91 dB when the source impedance Z_{opt} = 12.3 + j8.70 Ω and the load impedance Z_{ML} = 10.8 + j26.8 Ω. The corresponding power gain is equal to 12.96 dB. The schematic of the LNA including the input and output matching networks implemented with lumped elements is shown in Fig. 3.

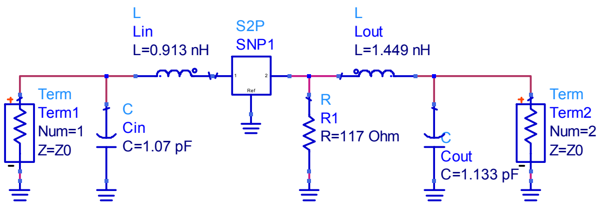

Fig. 3. Schematic of the LNA with synthesized matching networks: IMN{Cin= 1.07 pF, Lin =0.913 nH } and OMN{Cout=1.133 pF, Lout=1.449 nH}.

In this work, the design of the matching networks is done for the minimum noise figure, NF_{min}, hence no tradeoff between NF and power gain was done. Both the noise figure and the power gain meet the LNA specification.

LNA IMPLEMENTATIONS: SIMULATION RESULTS AND ANALYSIS

There are two possibilities to implement the previous LNA design: 1) using discrete passive components (i.e., lumped element models), and 2) using microstrip transmission lines (i.e., distributed element models). These two implementations are presented and analyzed below.

A. LNA Design I: Lumped IMN and OMN

Passive RLC components are nowadays small in size but for high precision at high frequency they become very expensive. Even for RF recommended components, tolerances are in the range of ±10 to ±30%, [3]-[4]. Another general problem when designing RF circuits implemented with discrete components is the general lack of high-frequency component models. The design process becomes more and more uncertain for small nominal component values used in RF applications. As shown in [2], the classical RLC model for capacitors must be replaced by sophisticated distributed models. All these aspects result in poor designs and low manufacturing yields. Therefore it is very interesting to simulate and analyze the LNA circuit shown in Fig 3 with appropriate components values together with their tolerances.

Fig. 4 illustrates the output noise figure variation when the IMN component nominal values vary accordingly to their data sheet [3-4]. Almost all simulated combinations within the specified component tolerances result in greater noise figure than the LNA specification permits.

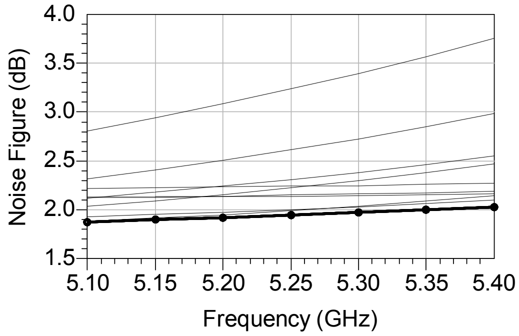

Fig. 4. Simulated noise figure when: Cin = 1.1 ±0.25 pF, Lin = 1.0 ±0.3 nH compared to the minimum noise figure (line marked with dots).

Fig. 5 shows that the matching networks are highly sensitive to the LNA power gain, as well. Note that the power gain can fall as low as 9 dB at 5.25 GHz and 8 dB at 5.35 GHz.

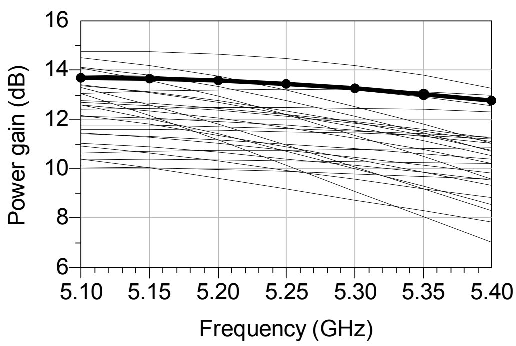

Fig. 5. Simulated power gain when Cin = 1.1 ±0.25 pF, Lin = 1.0 ±0.3 nH, Cout = 1.1 ±0.25 pF, Lout = 1.4 ±0.3 nH, compared to the nominal designed power gain (line marked with dots).

B. LNA Design II: Distributed IMN and OMN

The second design of the LNA, using microstrip lines and thus distributed models, is shown in Fig. 6. The microstrip IMN and OMN are synthesized in ADS using the PCB parameters listed in Table 1.

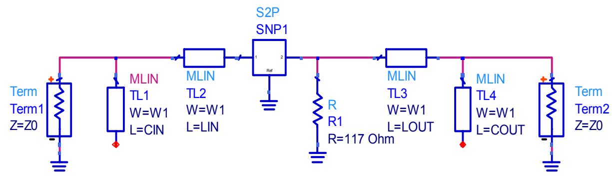

Fig. 6. Schematic of the LNA with microstrip line input and output matching networks.

The output noise figure and power gain, when the line width varies with ±10% and the dielectric constant of the substrate varies with 3.48 ± 0.05 are shown in Fig. 7 and Fig. 8, respectively.

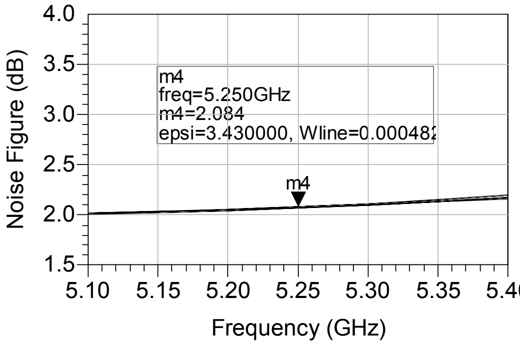

Fig. 7. Simulated noise figure when the microstrip line width varies with ±10% and the dielectric constant of the substrate varies with 3.48 ± 0.05.

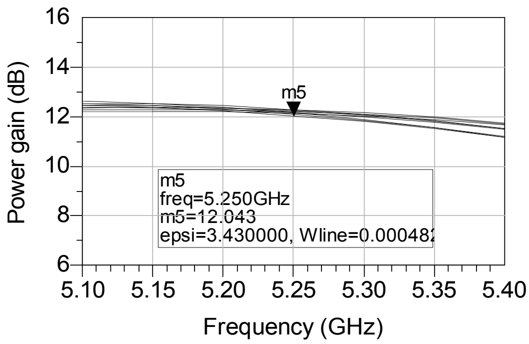

Fig. 8. Simulated power gain when the microstrip line width varies with ±10% and the dielectric constant of the substrate varies with 3.48 ± 0.05.

By comparing Fig. 7 to Fig. 4 and Fig. 8 to Fig. 5 it is apparent that a better control upon the LNA noise figure and power gain can be obtained when the microstrip line matching networks are used. The simulation results also show that the LNA performance meets the specification. Fig. 9 shows the LNA power gain simulation result with the microstrip IMN and OMN.

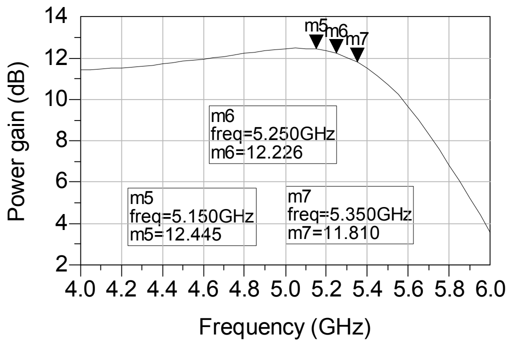

Fig. 9.Simulated power gain of the LNA with the microstrip IMN and OMN.

EXPERIMENTAL RESULTS

Samples of the LNA implemented with microstrip IMN and OMN were fabricated. Figs. 10a and b show the ADS layout and the photograph of the LNA test module, respectively.

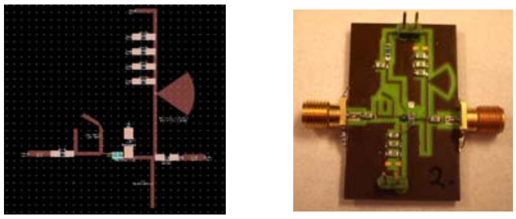

Fig. 10. LNA with microstrip IMN and OMN: (a) layout, and (b) processed test module.

Fig. 11 shows the measured power gain of the LNA. By comparing the simulated LNA power gain, shown in Fig. 9, to the measured one shown in Fig. 11, it can be seen that the LNA design based on distributed matching network models predicts the manufactured LNA performance very well.

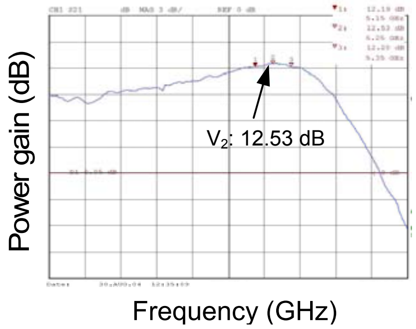

Fig.11. Mesured power gain of the LNA with the microstrip IMN and OMN

CONCLUSIONS

The agreement between simulated and measured power gain confirms that a good and predictable 5 GHz LNA design can be obtained when using microstrip lines as matching networks. Also important, the LNA noise figure and power gain are almost insensitive to microstrip line and process parameter variations.

On the contrary, the lumped element design of the LNA at 5 GHz has difficulties to achieve a high performance. Discrete passive components recommended for RF applications still have large tolerances of their nominal values. Sensitivity analyses have shown severe degradation of the noise figure and power gain of the LNA.

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[1] S. Gong, M. Karlsson, and A. Serban, "Design of a Radio Front End at 5 GHz", Proceedings of the IEEE 6th Circuits and Systems Symposium on Emerging Technologies, Vol. I, pp. 241-244, 2004.

[2] C. R. Sullivan, and A. M. Kern, "Improved Distributed Model for Capacitors in High-Performance Packages," Industry Application Conference, 2002. 37th IAS Conference, Oct. 2002.

[3] www.toko.com, chip inductors, type LL1005FH.

[4] www.murata.com, ceramic capacitors, type GJ61555C1HR75B.

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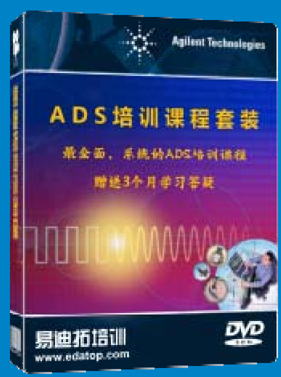

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